

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-218039

(43)Date of publication of application : 27.08.1993

(51)Int.Cl. H01L 21/321

(21)Application number : 04-019613 (71)Applicant : FUJITSU LTD

(22)Date of filing : 05.02.1992 (72)Inventor : HARADA SHIGEKI
MURATAKE KIYOSHI
MIZUKOSHI MASATAKA
KODAMA KUNIO

(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To prevent a short-circuit between bumps due to collapse of the bump in a semiconductor device having a flip chip structure in which a solder bump is used as an external connection terminal.

CONSTITUTION: The semiconductor device comprises a flip chip structure in which a solder bump 5 is used as an external connection electrode in such a manner that a part except an end 5P contributing to the fixture of the bump 5 to an external conductor is buried in a heat resistant resin film 12 having rigidity and coating a bump 5 arranging surface of the chip.

CLAIMS

[Claim(s)]

[Claim 1]A semiconductor device characterized by coming to be embedded in a heat-resistant-resin film which has the flip chip structure which uses a solder bump as an external connection electrode and in which it has the rigidity applied to a vamp allocation side of this chip except a tip part which contributes to adherence with this solder bump's outer conductor.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the semiconductor device of the flip chip structure which uses a solder bump as an external connection terminal.

[0002] The semiconductor device of flip chip structure with which face down bonding is made via a solder bump on the circuit board. Although a bonding process is simplified and connection resistance with large bond strength with easy automation is coming to be recently used abundantly from an advantage like it is small. The number of bumps increases with large-scale high integration of the circuit allocated by the semiconductor chip and a bump interval also narrows and the short circuit accident between the bumps generated after bonding is actualizing. An improvement is desired.

[0003]

[Description of the Prior Art] Drawing 5 is a mimetic diagram of an example of the flip chip structure semiconductor device (it is henceforth called a flip chip for short) of the conventional solder bump method and is (a). A top view and (b) A bump region disposing sectional view and (c) A bump part expanded sectional view and drawing 6 are the type section figures showing the mount condition to the wiring board top.

[0004] (a) of drawing 5 (b) And (c) So that it may be shown the flip chip of the conventional solder bump method. The surface-protection film 2 which consists of silica glass etc. is formed on the semiconductor chip 1 in which the integrated circuit (not shown) etc. were formed. The contact window 3 which expresses aluminum (aluminum) wiring (not shown) of the request on the semiconductor chip 1 on this surface-protection film 2 is formed. It had the structure where the solder bump 5 which the chromium (Cr) layer 4a, the copper (Cu) layer 4b and the golden (Au) people 4c become from a lead (Pb)-tin (Sn) alloy via the barrier metal layer 4 which it comes to laminate one by one was welded from the lower layer on this contact window 3.

[0005] And the flip chip of such a solder bump method. As shown in the type section figure of drawing 6, this flip chip 56 is changed into a facedown state. For example, on the wiring boards 7 such as a ceramic package, alignment of the electrode 8 and the solder bump 5 who were formed in the 7th page of the wiring board and by whom Au plating or solder plating was done is carried out. They are carried and adherence loading is made by carrying out

a reflow of the solder bump 5 with a heating furnace etc.

[0006]

[Problem(s) to be Solved by the Invention] Since the performance degradation by the rise of chip temperature will on the other hand produce the semiconductor device of flip chip structure if the number of semiconductor devices carried with expansion of circuit structure increases in order to suppress the rise in heat of the above-mentioned chip a radiation fin adheres to the back of a flip chip.

[0007] After adherence of the radiation fin in that case carries the flip chip 56 and adheres on the wiring board 7 (refer to drawing 6) in order to be made by soldering to the chip back which has Au vacuum evaporation film and to decrease the thermal resistance between a chip and a fin where a pressure is applied it is performed.

[0008] Therefore in [as shown in the type section figure which shows the problem of drawing 7] said conventional flip chip 56 The solder bumps for example 5A and 5B which adjoin when the solder bump 5 is crushed it expands to a transverse direction and the allocation density of a vamp increases by heating and application of pressure at the time of soldering the radiation fin 9 on Au vacuum evaporation film 10 on the back of a chip (11 is a soldering part) are short circuits (S). The problem of carrying out is produced.

[0009] Then an object of this invention is for an external connection terminal to prevent the short circuit between vamps by vamp crushing of the semiconductor device (flip chip) of the flip chip structure which consists of solder bumps.

[0010]

[Means for Solving the Problem] Solution of an aforementioned problem has the flip chip structure which uses a solder bump as an external connection electrode and is attained by semiconductor device by this invention which it comes to embed in a heat-resistant-resin film in which it has the rigidity applied to a vamp allocation side of this chip except a tip part which contributes to adherence with this solder bump's outer conductor.

[0011]

[Function] Drawing 1 is a type section figure for principle explanation of this invention. The flip chip type semiconductor device (flip chip) of the solder bump method which starts this invention as shown in this figure The solder bump 5 is welded via the barrier metal layer 4 by the surface-protection film 2 of glassiness which covered the semiconductor chip 1 top in which the integrated circuit etc. were formed and was laminated on the contact window 3 provided so that wiring of the request

on the semiconductor chip 1 which is not illustrated might be expressed. And it has the structure where the lower region except the tip part 5P which contributes to welding with the solder bump's 5 outer conductor was embedded in the heat-resistant-resin film 12 which has rigidity.

[0012]Thereforecrushing of the vamp 5 at the time of carrying out face down bonding of this flip chip to an outer conductor by the solder bump's 5 reflow is stopped by the tip part 12P of the heat-resistant-resin film 12 which is burying the solder bump's 5 circumferenceAnd after adhering a chip on a wiring boardcrushing of the solder bump 5 by heating and application of pressure at the time of attaching a radiation fin to the back of this chip by soldering does not attain to the portion below the tip part 12P of said heat-resistant-resin film 5 againeither. Thereforethe solder bump 5 does not spread greatly in a transverse direction by the solder bump's 5 crushingand the adjoining short circuit accident between solder bumps is prevented.

[0013]

[Example]With reference to the manufacturing process sectional view showing the flip chip structure semiconductor device (flip chip) of the solder bump method which starts this invention below in drawing 2 and drawing 3 about one exampleand the type section figure showing the mount condition shown in drawing 4it explains concretely.

[0014]Drawing 2 (a) It faces forming the semiconductor device concerning reference above-mentioned this inventionThe integrated circuit etc. which are not illustrated as usual the principal surface top in which said integrated circuit of the formed semiconductor substrate 101 is formed on the surface-protection film 2 of a wrapfor examplea silica glass system about 1 micrometer thick. By the photolithography technique using a well-known dry etching meansit is the semiconductor substrate 101. Two or more contact windows 3 which express separately the wiring surface of two or more upper requests that are not illustrated are formed. Au vacuum evaporation film 10 used for radiation-fin attachment etc. is beforehand formed in the back of the semiconductor device substrate 101 as usual.

[0015]Drawing 2 (b) Like subsequently the formerfrom a lower layer one by one by a sputtering technique 3 ** to the principal surface top of the above-mentioned semiconductor substrate 101i.e.the inner surface of the above-mentioned contact window 3 and the upper surface of the surface-protection film 2a Cr layer about 1000Å thickA Cu layer about 1000Å thick and an Au layer about 5000Å thick form the barrier metal layer 4 which it comes to laminate one by one.

[0016]Drawing 2 (c) Etching removal of the above-mentioned barrier metal layer 4 is selectively carried out with the well-known photolithography technique using a dry etching means like subsequently the former 3 **The wrap barrier metal pattern 4P is formed for the inner surface of the contact window 3 and its periphery by predetermined width on the contact window 3 of the surface-protection film 2. The gas of a chlorine (Cl) system is used for etching gas.

[0017]Drawing 2 (d) It is the thickness of a 60 lead (Pb) / 40 tin (Sn) presentation selectively on the above-mentioned barrier metal pattern 4P by the mask deposition means of for example common knowledge like subsequently the former 3 **for example. The about 150-micrometer solder pattern 105 is formed.

[0018]Drawing 2 (e) Subsequently it is in a vacuum or inactive gas about this semiconductor substrate 101 3 **. It heats at about 400 **a reflow of said solder pattern 105 is carried out and the spherical solder bump 5 is formed.

[0019]Drawing 3 (a) In order to form the flip chip concerning reference this invention After finishing the above conventional flip chip formation process the polyimide resin 112 which is heat resistant resin is applied to the upper surface of the substrate with which the above-mentioned solder bump 5 adhered with a spin coat method at a thickness of about 50 micrometers Where a spreading side is turned upwards it heats at about 80 ** for example in inactive gas for about 1 hour and precure of the above-mentioned polyimide resin film 112 is performed. The polyimide resin film 112 of the solder bump's 5 upper part flows and falls to a periphery into this precure and the thickness (t) of the periphery which touches the solder bump 5 is set to about 100 micrometers. The thickness of the polyimide resin film 112 the solder bump's 5 tip end part becomes thin at about several micrometers in this case.

[0020]Drawing 3 (b) Subsequently 3 ** by for example the dry etching means using the mixed gas of oxygen (O_2) and 4 fluoridation carbon (CF_4). The above-mentioned polyimide resin film 112 is etched until the solder bump's 5 tip part 5P projects in the height which is about 50 micrometers subsequently to about 400 **this substrate is heated for example in inactive gas for about 1 hour and the after-cure of the polyimide resin film 112 is performed. The polyimide resin film 112 turns into a film which fully has rigidity here.

[0021]Drawing 3 (c) Subsequently the usual dicing means divides the above-mentioned semiconductor substrate 101 for every semiconductor chip 3 **and the flip chip 6 of the solder bump method concerning this invention is completed.

[0022] Thus polyimide film 112 whose lower region except the tip part 5P which the flip chip 6 concerning formed this invention contributes to welding with the solder bump's 5 outer conductor is a heat-resistant-resin film which has rigidity It has the structure embedded inside.

[0023] Therefore as shown in drawing 4 the above-mentioned flip chip 6 is changed into a facedown state For example on the wiring boards 7 such as a ceramic package carry out alignment of the electrode 8 and the solder bump 5 who were formed in the 7th page of the wiring board and by whom Au plating or solder plating was done and they are carried Crushing of the solder bump 5 for [although not illustrated in the case] heating and application of pressure in the case of radiation-fin soldering after loading which carried out adherence loading by carrying out a reflow of the solder bump 5 with a heating furnace etc. It is restricted only to the tip part projected from the polyimide film 112 which has the rigidity which is embedding this vamp 5 and the solder bump 5 is crushed greatly and does not spread greatly in a transverse direction. Therefore also when a solder bump's allocation density increases the short circuit accident of the adjoining solder bumps in the above-mentioned process is prevented.

[0024]

[Effect of the Invention] according to this invention in the flip chip structure semiconductor device of a solder bump method a solder bump's crushing can be minutely suppressed at the time of heating boiled and depended on the radiation-fin attachment the time of loading of the flip chip to a wiring board top and after loading etc. and application of pressure like explanation above. Therefore this invention largely contributes to improvement in the reliability at the time of loading of the flip chip structure semiconductor device of the solder bump method with which circuit structure was expanded and the allocation density of the vamp increased.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The type section figure for principle explanation of this invention

[Drawing 2] manufacturing process sectional view (the 1) concerning one example of the semiconductor device of this invention

[Drawing 3] manufacturing process sectional view (the 2) concerning one example of the semiconductor device of this invention

[Drawing 4]The type section figure showing the mount condition of the semiconductor device concerning this invention

[Drawing 5]The mimetic diagram of the conventional flip chip

[Drawing 6]The type section figure showing the mount condition of the conventional flip chip

[Drawing 7]The type section figure showing the problem of the conventional flip chip

[Description of Notations]

1101 semiconductor chips

2 Surface-protection film

3 Contact window

4 Barrier metal layer

5 Solder bump

5P solder bump's tip part

6 and 56 Flip chip

7 Wiring board

8 Electrode

9 Radiation fin

10 Au vacuum evaporation film

11 Soldering part

12 Heat-resistant-resin film

The tip part of 12P heat-resistant-resin film

112 Polyimide film
